# PAGING IN ORACLE SPARC SOLARIS

## MEMORY MANAGEMENT ARCHITECTURE

OPERATING SYSTEMS PRESENTATION

# WHAT IS SPARC?

***Scalable Processor Architecture***

- RISC architecture by Sun (now Oracle)
- 64- bit processor with advanced features
- Designed for high-performance computing
- Known for reliability and scalability

**KEY FEATURE:**
**Hardware memory management with MMU**

# SOLARIS OPERATING SYSTEM

# ENTERPRISE UNIX OS

- Unix-based operating system optimized for SPARC
- Advanced virtual memory management
- Support for multiple page sizes
- Dynamic memory optimization features

**Solaris implements sophisticated demand paging with hardware-software cooperation**

# VIRTUAL MEMORY FUNDAMENTALS

**Benefits**

- **Process isolation**
- **Memory protection**
- **Efficient memory use**
- **Large address spaces**

## CORE CONCEPTS

- VIRTUAL ADDRESS SPACE: each process has its own virtual memory
- PHYSICAL MEMORY: actual RAM in the system
- PAGES: fixed-size memory blocks
- PAGING: mapping virtual pages to physical frames

# SPARC MMU ARCHITECTURE

## HARDWARE MEMORY MANAGEMENT

The SPARC MMU provides hardware support for virtual-to-physical address translation

### Components

- Translation Storage Buffer (TSB)
- TLB (Translation Lookaside Buffer)
- Page Table Walkers

### Features

- Multiple page sizes
- Separate I -TLB & D-TLB
- Hardware page table walk

# PAGE TABLE STRUCTURE

| Level | Component | Size |
|---|---|---|
| 1 | Context table | 512 entries |
| 2 | Region/ Segment | Variable |
| 3 | Page Table (PTE) | Points to frames |

```
LEVEL 1: context table (512 entries)
```

```
LEVEL 2: region/segment tables
```

```
LEVEL 3: page table entries (PTEs)
```

SPARC V9 uses a three-level page table hierarchy for efficient address translation

# TRANSLATION LOOKASIDE BUFFER (TLB)

## HIGH-SPEED ADDRESS TRANSLATION CACHE

TLB caches recent virtual-to-physical address translation for fast memory access

SPARC TLB Features

- Separate instruction and data TLBs
- Fully associative design
- Typically 64-512 entries
- Hardware-managed on most models

PERFORMANCE IMPACT

TLB Hit: ~ 1 clock cycle

TLB Miss: 10-100+ cycles

- Critical for performance

| STEP | ACTION | RESULT |
| --- | --- | --- |
| 1 | Virtual Address | Generated by CPU |
| 2 | Check TLB | Hit or Miss |
| 3a | TLB Hit | Get physical address |
| 3b | TLB Miss | Walk page tables |
| 4 | Update TLB | Cache translation |
| 5 | Access Memory | Use physical address |

# ADDRESS TRANSLATION PROCESS

## TRANSLATION STEPS

1. CPU generates address
2. Check TLB
3. On miss, walk tables
4. Update TLB

# MULTIPLE PAGE SIZES

## FLEXIBLE MEMORY MAPPING

SPARC/Solaris supports multiple page sizes for optimized memory usage

**SUPPORTED PAGE SIZES**

8 KB- Standard page
64 KB- Medium page
512 KB- Large page
Up to 256 MB on some models

**BENEFITS**

- Reduced TLB misses
- Better memory efficiency
- Improved cache performance
- Optimized for workload

# PAGE FAULT HANDLING

## WHEN PAGES ARE NOT IN MEMORY

Page faults trigger when accessing unmapped or swapped-out pages

### Fault Types

**MINOR: Page in memory, not in TLB**

**MAJOR: Page on disk, must load**

**INVALID: Access violation**

## RESOLUTION STEPS

- Hardware traps to OS
- Locate page (disk or memory)
- Load page if needed
- Update page tables
- Resume execution

Solaris uses efficient page replacement algorithms (CLOCK, NFU) to minimize page faults

# PERFORMANCE OPTIMIZATION FEATURES

**HARDWARE OPTIMIZATIONS**

- Fast hardware page table walks
- Large TLB capacity
- Multiple page size support
- Prefetching mechanisms

**SOFTWARE OPTIMIZATIONS**

- Adaptive page sizing
- Memory pressure management
- Copy-on-write optimization
- Shared memory support

**KEY FEATURES**

**TSB:** Translation Storage Buffer caches translations

**ISM:** Intimate Shared Memory for efficient sharing

**DISM:** Dynamic ISM for flexibility

# SUMMARY: SPARC SOLARIS PAGING

KEY TAKEAWAYS

- SPARC provides robust hardware support for virtual memory
- Three –level page table hierarchy enables efficient translation
- TLB is critical for high-performance memory access
- Multiple page size optimize different workloads
- Hardware-software cooperation achieves excellent performance

**SPARC/SOLARIS DEMONSTRATES ENTERPRISE-GRADE MEMORY MANAGEMENT WITH ADVANCED PAGING FEATURES**

# THANK YOU

Marina Skegro